1,090,112

PATENT SPECIFICATION 1,090,112

DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Improvements in or relating to Pulse Transmission Systems.

I, HER MAJESTY'S POSTMASTER GENERAL, of The General Post Office, London, E.C.1, do hereby declare the invention, for which I pray that a patent may be granted to me, and the method by which it is to be performed, to be particularly described in and by the following statement:—

In pulse transmission systems, in particular multi-channel pulse code modulation systems, it is usual to insert digital regenerative repeaters at regular intervals in the signal transmission path, these being powerfed over the transmission path. For this reason, and also because the path may be a balanced pair and the repeater unbalanced, it is necessary to insert a transformer at the signal input to the repeater. In consequence, the d.c. component of the signal is lost. All the problems of a "wandering zero", well known in telegraphy and data transmission, have therefore to be faced. D.C. restoration circuits are an undesirable complication, and the alternative of arranging that the line signal contains little or no energy at zero or very low frequencies is usually preferred. One method is to use a method of signal transmission variously known as bipolar, alternating binary, or alternate mark inversion. In this method, a space is represented by no signal and a mark by either a positive pulse or a negative pulse, these latter occurring alternately. That method requires a repeater capable of detecting and repeating three-condition or ternary signals.

Another method is to transmit binary signals, but to restrict the combinations of digits which are used to these which have a low disparity, i.e. only a small marking or spacing bias. One such system intended for pulse code modulation of speech, uses groups of nine digits in which there is a maximum of either 5 marks and 4 spaces or 4 marks and 5 spaces, and is called therefore a unit-display code. This gives 252 usable combinations nearly as many as an unrestricted 8-binary-digit system which provides a total of 256 usable combinations. However, if this system has to be interconnected with another link which will accept relatively unrestricted binary signals, a code converter must be inserted, to convert unrestricted binary digits to unit-disparity code digits. Furthermore, since 252 is less than 256, it is not possible to convert all unrestricted 8-binary-digit combinations to unit-disparity 9 code digit combinations.

Even if all pulse code modulation systems use unit-disparity code, the problem of code conversion will still arise if it is desired to accept, for transmission over the system, digital data in unrestricted binary code form.

According to the present invention a pulse code transmission system for binary digital signals, for example, pulse code modulation signals, includes a transmitter having a converter for receiving groups of unrestricted binary code signals, means for determining on a cumulative basis the disparity value of each group, inverting the polarity of each code digit signal in a group if the disparity value of the inverted polarity group reduces the integrated disparity values of the preceding groups but not otherwise and adding a further digit position for receiving a signal coded on a binary basis to indicate whether the polarity of the group has been inverted, and transmitting the groups, and a receiver for receiving the transmitted groups and including a device for examining the further digit position and sensing the binary value of the signal there-

[*Price*

in and for restoring to their original polarity the code digit signals of each inverted polarity group.

The converter may comprise a store in which the code digits of each received group are temporarily stored.

Preferably, the further code digit position is added at the beginning of each group transmitted by the transmitter. The binary coding used for the signal in the further digit position may be a polarity coding, i.e. a mark or a space or a presence-absence coding.

The groups transmitted by the transmitter may be retimed to permit the addition of the further code digit position so that if the received groups of unrestricted binary code signals contain n code digits, the transmitted groups contain space for $n + 1$ digits, the total duration of the received and transmitted groups being the same. Similarly at the receiver, retiming to accommodate a change from $n + 1$ to n digits may be desirable.

The code used in the invention gives low disparity, although not over such a short period of time as the unit-disparity code. The code used in the invention has the advantage that conversion from and to unrestricted binary is much simpler.

By way of example only, a system embodying the invention for converting a sequence of 8-binary-digit unrestricted code signals into a sequence of 9 digit signals whose integrated disparity is low will now be described in greater detail with reference to the accompanying drawings of which:—

Fig. 1 shows, in block schematic form only, the transmitting terminal of the system,

Fig. 2 shows, in block schematic form only, the receiving terminal of the system, and

Fig. 3 is a pulse timing diagram.

8-digit code signals to be transmitted are applied to the input of a converter in the transmitter at a speed of C characters (i.e. groups of unrestricted binary digits) per second. Two streams of sampling pulses are used in the converter, one of which has a pulse repetition rate of 8C pulses per second and is designated P8 while the other pulse stream has a pulse repetition rate of 9C pulses per second and is designated P9. The P8 pulses are derived either from the device (no shown) which generates the stream of binary input digits, or, by well known means, from the converter input stream and are timed to occur coincidentally with the digits of an 8-digit signal. The converter requires two further pulse streams designated P1.1 and P1.2, the pulses of which occur once per character. The P1.1 pulses occur before the P1.2 pulses, but both occur in the interval between two P9 pulses which coincides with the end of a character.

For convenience, it is proposed to attribute to the mark and space conditions of the binary signals the values +1 and −1 respectively. Thus, the disparity of an 8-digit code signal may lie between +8 if the signal contains 8 marks and −8 if the signal contains 8 spaces. Other possible disparity values are −6, −4, −2, 0, 2, 4 and 6.

The 8-digit code signals are applied to the input of an 8-stage shift register indicated by block 1. The register is of well-known form and may comprise, for example, a chain of trigger circuits. Each stage of the register has a connection to a character disparity unit indicated by block 2. Connection is made at a point in each stage at which the potential will indicate the polarity (i.e. +1 or −1) of the digit stored in the stage.

Let it be assumed that the potential of the point will, except when digits are being transferred from stage to stage, be +V1 when the stored digit is +1, and of a different value +V2 when the stored digit is −1. The points on the stages of the shift register are joined via resistors 3 to a common point 4 itself joined by a resistor 5 to a potential +V2. Resistors 3 are of equal resistance which is equal to that of resistor 5. A further resistor 3 is connected permanently to a source of potential +V1. Point 4 is connected to the input of a linear gate 6 which is opened by pulses P1.2 to allow the potential at point 4 to be fed to an Eccles-Jordan trigger circuit represented by block 6A.

The voltage of point 4 depends upon the disparity of the code signal stored in the shift register. If four or more of the stages of the register contain +1 digits, the potential of point 4 will be between V1 and $\frac{V1 + 2V}{2}$. If fewer than four stages contain +1 digits, then the potential of point 4 will be between V2 and $\frac{V1 + V2}{2}$.

The Eccles-Jordan trigger circuit 6A is arranged to give an output condition of +1 when the potential of point 4 is between V1 and $\frac{V1 + V2}{2}$ and an output condition of −1 when the potential of point 4 is between V2 and $\frac{V1 + V2}{2}$.

The output of trigger circuit 6A forms one of the two inputs to a multiplier represented by block 7. The other input to the multiplier 7 is received from an integrator indicated by block 8. The integrator includes a counter which steps forward when

a digit of mark polarity (+1) is applied to it and backward when a digit of space polarity (−1) is applied to it. The input to the counter comprises a stream of digits appearing on lead 9 and thus the counter indicates at any one moment the total disparity of digits which have appeared on lead 9 up to the moment. It will be apparent from what follows that the counter cannot exceed a total forward or backward movement of 13 indicating respectively a total positive disparity of +13 or a total negative disparity of −13.

The integrator is arranged to provide an output condition of +1 when the total disparity recorded by the counter is positive and an output condition of −1 when that total is negative. If the total disparity is zero, it is desirable that both conditions are equiprobable and it is preferred that the outputs remain at the condition reached immediately previous to zero disparity being indicated on the counter. Thus the output condition for zero disparity will be −1 if the immediately previous disparity had been negative or +1 if that disparity had been positive.

The inputs to multiplier 7 are combined in such manner that inputs of like condition cause the multiplier to generate an output condition of +1 whilst unlike inputs produce an output condition of −1.

The output of multiplier 7 is applied as an input to a trigger circuit 10 which delivers an output signal of −1 when the input signal is +1, and an output signal of +1 when the input signal is −1. This output is fed to multiplier 11.

Each stage of the shift register 1 is connected via gate to a corresponding stage in a nine stage shift register 12. All the gates are controlled by a comon pulse lead carrying the P1.1 or the P1.2 pulses. The ninth stage, designated I, of register 12 is placed ahead of that stage corresponding to stage number 1 of the register 8. The pulse lead is connected directly to the additional stage so that the same digit condition is written into this stage at each occurrence of a gating pulse. The shift register 12 is stepped by the P9 pulses, operating through a delay element indicated by block 14 which introduces a delay of a small fraction of a P9 pulse duration. The output of the register is passed via a linear gate 13 opened by P9 pulses to the multiplier 11. The output of multiplier 11 appears on lead 9 which is connected via a line transmit unit shown as block 15 to an output circuit 16. The line transmit unit converts the signals on lead 9 to a form appropriate to the nature of the circuit 16. For example, if circuit 16 is a line circuit the pulses on lead 9 may be converted into telegraph signals.

The manner of operation of the converter will now be described, it being assumed that an 8-digit code signal of disparity −4 is being received, and that the total disparity already reached is negative.

The 8-digit signal is stored in the shift register 1 and its disparity examined in the manner described above by the character disparity unit 2. The signal is found to have a disparity of −4 giving a net disparity of −3 as seen at point 4, so that the potential of point 4 is between V2 and $\frac{V1 + V2}{2}$ and the trigger circuit 6A applies to multiplier 7 the condition of −1, at the time of occurrence of the P1.2 pulse. Just before this occurs, trigger 10 has been reset by pulse P1.1.

Integrator 8 has reached a disparity count such that the condition applied to multiplier 7 from the integrator is also −1 and thus the output condition of multiplier 7 is +1. That condition is transmitted, at the instant of occurrence of the P1.2 pulse to trigger circuit 10 which transmits a −1 condition to multiplier 11.

The 8-digit code stored in shift register 1 is transferred in parallel at time P1.1 or P1.2 to the shift register 12 and at the same time an additional digit, always of the same polarity, is written into the additional stage I. The contents of register 12 are read out by the ensuing frame of P9 pulses, via the linear gate 13 to the multiplier 11. The added digit in stage I of register 12 is the first to be read out and is followed by the remaining eight in the same order as that in which they are received by shift register 1. Because a signal −1 exists on the other input lead to the multiplier 11, the signals fed into it from linear gate 13 will appear on lead 9 in inverted form and will be so transmitted to the output circuit 16 via unit 15. Because the disparity of the received character was negative that of the transmitted character will be positive, thus tending to reduce the cumulative disparity. The transmitted signal is fed also to integrator 8 thereby causing output of the latter to be adjusted to correspond with the sense of the new cumulative disparity.

It will be appreciated that while the digits of an 8-digit character are being received in shift register 1 the digits of the preceding character, themselves preceded by the additional indicating digit, are being read out of shift register 12. Thus the device introduces a delay of one character period.

The presence of the added digit from stage I of register 12 indicates that the polarity of the digits forming the following signal have been inverted and is used in a receiving terminal now to be described to effect a re-inversion where necessary.

Line signals are received by a line receive unit represented by block 17 which derives from the received signals, in known manner, streams of pulses P9 and P9.1 for regenerating the digits. The regenerated pulses are transmitted to a linear gate 18 and a multiplier indicated by block 19. Linear gate 18 is controlled by the initial pulse P9.1 only of each frame of P9 pulses and the gate therefore opened to pass to the trigger 20 the polarity of the indicating digit of each group of character digits. Trigger 20 is so arranged that if the polarity of the indicating digit fed to it indicates that reversal has been effected at the transmitter, it feeds a negative signal to a multiplier 19. This signal persists until the state of trigger 20 is reversed by some later indicating digit, and it causes the signals appearing at the output of multiplier 19 to be opposite in polarity to those at its input. Thus the original polarity of the signals has been restored. The signals are passed to a linear gate 21 which is opened at each character digit time but is closed at indicating digit time so that only the character digits are passed to pulse store 22. The signals may be read out from the store and applied to a decoder (not shown) or, if they are to be transmitted onwards as unrestricted binary digit signals they are read out by pulse train having eight pulses per character.

The system has been described with reference to a group of 8 unrestricted binary digits. The principle can be applied to a group of any number of digits, but the input binary stream must have a "frame" (as a pulse code modulation system has) and the number in the group must be simply related to the frame, in order that the position of the control digits can be identified. This is most easily achieved, as in the above case, by making the group equal to the number of digits in a time slot, i.e. equal to the number of digits in a time slot, i.e. equal to the number of coding and signalling digits of a channel.

The system has another possible advantage when time division multiplex electronic exchanges are used. It is convenient to have a spare digit time period after each time slot, to give time for switching operations within the exchange. This can be provided easily with the proposed system by not retiming the received signals with a slower clock as described above. The 9th digit period will then remain, and will provide the switching time required for the exchange. At the outgoing side of the exchange the control digit required for the next transmission link, (assuming that this link is also working with the low disparity system described) can be inserted in the 9th digit position, so that no retiming with a faster clock is necessary at this point.

With this code, a nine-digit group can give disparity values of 1, 3, 5, 7 or 9, in each case either plus or minus (marking or spacing), and changing the sign of the control digit will merely reverse the sign of the disparity. Since each group will always (as the system has been described) reduce the accumulated disparity existing at its commencement, it follows that the maximum possible accumulated disparity is 9, produced when a 9-disparity group follows zero accumulated disparity. The condition under which this disparity will take longest to be reduced to zero is when the group giving a disparity of 9 is followed by a succession of groups with a disparity of 1. 9 such groups would be required to reduce the disparity to zero. This is the factor which will determine the lowest frequency for which the input transformers of the repeaters must be designated.

WHAT I CLAIM IS:—

1. A transmission system for binary coded digital signals comprising in combination, a transmitter having an input to which groups of unrestricted binary coded signals are applied, an output on which appear groups of restricted binary coded signals corresponding to said unrestricted groups, and, in said transmitter, a signal converter by which said unrestricted groups are received, a disparity valuing circuit in said converter for determining the disparity value of each group of said unrestricted groups, a second disparity valuing circuit for summing the disparity value of said restricted groups appearing on said output, a polarity inverting circuit in said converter for inverting the polarity of each digit of an unrestricted signal group in the event only that the disparity value of said group of inverted polarity when added to said summed disparity values reduces the latter, means for transmitting a further digit with each restricted signal group which indicates if the polarity of the group has been inverted, and a receiver having an input to which groups of signals appearing at said transmitter output are applied, said receiver including digit sensing means for sensing said further digit, and polarity restoring means connected to said digit sensing means for restoring the polarity of any received signal group including a further digit.

2. A transmission system for binary coded digital signals comprising in combination, a transmitter including a signal store for temporarily storing in succession each group of binary coded signals to be transmitted, a first disparity valuing circuit connected to said store for determining the disparity value of a stored group, a polarity inverting circuit connected to receive signals from said store to invert the polarity

of each digit of selected groups from said store, a digit adding circuit in said store, an output lead connected to said polarity inverting circuit, a second disparity valuing circuit for summing the disparity values of groups of signals appearing on said output lead, disparity value comparing means connected to said first and second disparity valuing circuits and for rendering operative said polarity inverting circuit only in the event that the disparity value of said stored signal increases the summed disparity values, said disparity comparing means also causing said digit adding circuit to add a polarity inversion indicating digit to each said selected group, and a receiver comprising digit sensing means for sensing said polarity inversion indicating digit, and polarity restoring means connected to said sensing means for restoring the polarity of each said selected group.

3. A transmission system as claimed in claim 2 and further comprising, in said signal store, a first shift register connected to receive, in succession, said groups of binary coded signals and having a number of stages equal to the number of digits in said groups, a second shift register having stages corresponding to the stages of said first register and an additional stage, a transfer circuit interconnecting each stage of said first register with the corresponding stage of said second register for transferring digits stored in said first register to said second register, said additional stage in said second register comprising said digit adding circuit, a transfer initiating lead connected to said transfer circuit and a read-out control lead connected to said second shift register.

4. A transmission system as claimed in claim 1 and further comprising, in said receiver, a receive unit connected to receive said groups of signals appearing at the output of said transmitter, gating means connected to the output of said receive unit to gate into said digit sensing means said further digit, and, connected to the output of said polarity restoring means, further gating means to gate out said further digit.

5. A transmission system comprising in combination a transmitter as described herein with reference to Fig. 1 of the accompanying drawings and a receiver as described herein with reference to Fig. 2 of the accompanying drawings.

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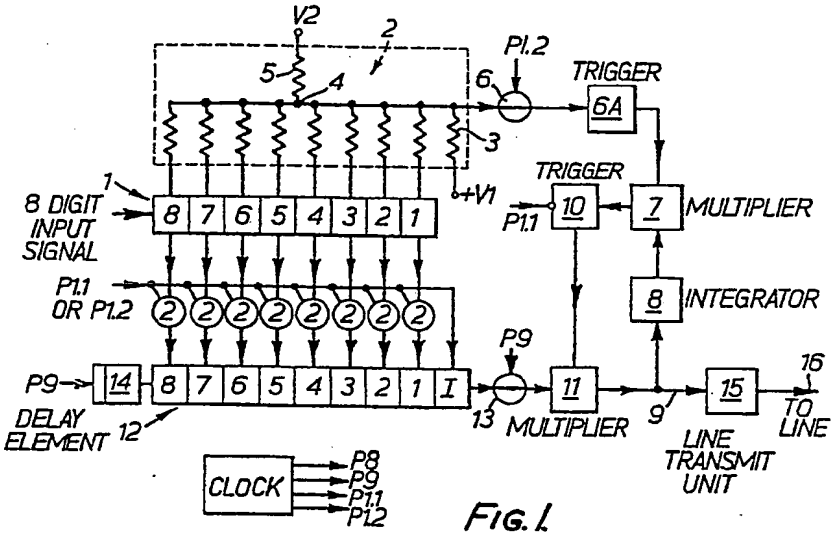

FIG. 1.

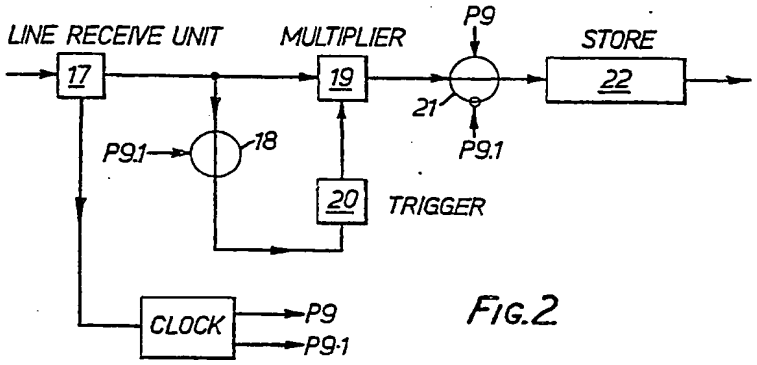

FIG. 2.

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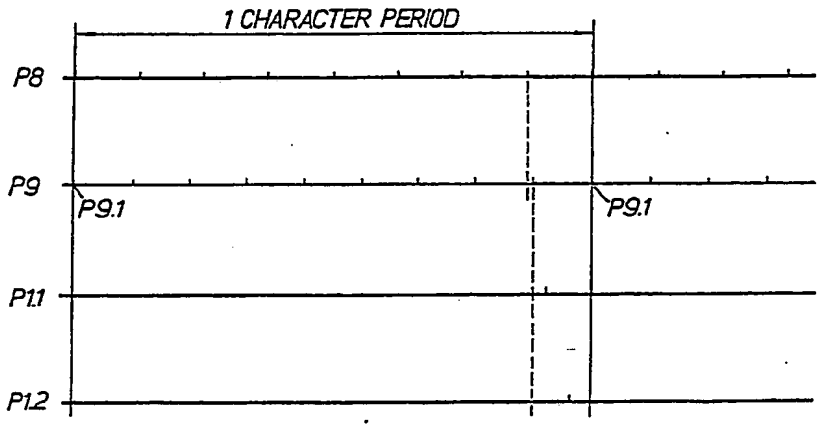

FIG. 3.

1090112 COMPLETE SPECIFICATION
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Sheets 1 & 2

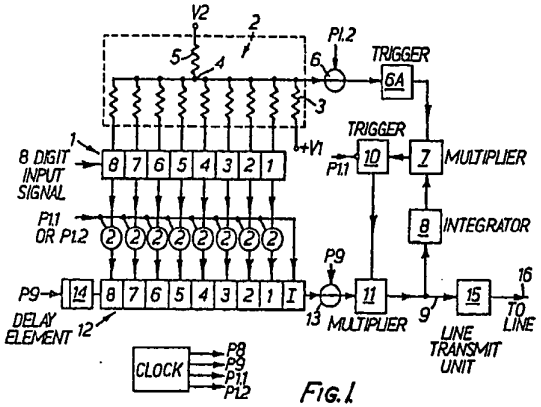

FIG. 1.

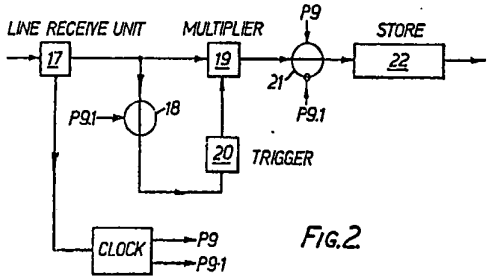

FIG. 2

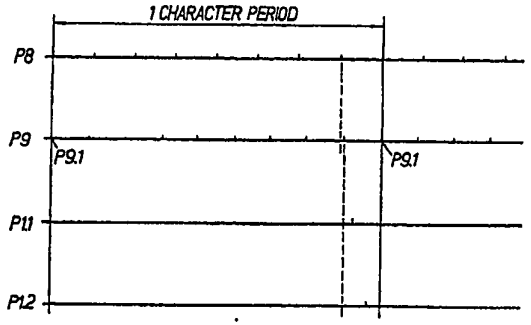

FIG. 3.